S5K3L6XX

1/3" 13M CMOS Image Sensor

Revision 0.01
Sept 2017

Data Sheet

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1. Wear antistatic clothes and use earth band.
2. All objects that are in direct contact with devices must be made up of materials that do not produce static electricity.
3. Ensure that the equipment and work table are earthed.
4. Use ionizer to remove electron charge.

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Do not use semiconductor products in an environment exposed to dust or dirt adhesion.

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Semiconductor devices are sensitive to:

- Environment
- Temperature
- Humidity

High temperature or humidity deteriorates the characteristics of semiconductor devices. Therefore, do not store or use semiconductor devices in such conditions.

Mechanical Shock

Do not to apply excessive mechanical shock or force on semiconductor devices.

Chemical

Do not expose semiconductor devices to chemicals because exposure to chemicals leads to reactions that deteriorate the characteristics of the devices.

Light Protection

In non- Epoxy Molding Compound (EMC) package, do not expose semiconductor IC to bright light. Exposure to bright light causes malfunctioning of the devices. However, a few special products that utilize light or with security functions are exempted from this guide.

Radioactive, Cosmic and X-ray

Radioactive substances, cosmic ray, or X-ray may influence semiconductor devices. These substances or rays may cause a soft error during a device operation. Therefore, ensure to shield the semiconductor devices under environment that may be exposed to radioactive substances, cosmic ray, or X-ray.

EMS (Electromagnetic Susceptibility)

Strong electromagnetic wave or magnetic field may affect the characteristic of semiconductor devices during the operation under insufficient PCB circuit design for Electromagnetic Susceptibility (EMS).

Revision History

Revision No.	Date	Description	Author(s)
0.00	July. 18, 2017	• Initial draft	JH Shin
0.01	Sept. 27, 2017	• Update typical digital supply power value	JH Shin

Table of Contents

List of Figures

List of Tables

List of Conventions

Register RW Access Type Conventions

Type	Definition	Description
R	Read Only	The application has permission to read the Register field. Writes to read-only fields have no effect.
RW	Read/Write	The application has permission to read and writes in the Register field. Written value effects on the next frame.
RW/R	Read/Write	The application has permission to read and writes in the Register field. Written value effects only on exit from stand-by.
RW/C	Read/Write	The application has permission to read and writes in the Register field. Changing value typically causes configuration change (either in abort timing or preserve timing modes).
RW/SR	Read/Write	The application has permission to read and writes in the Register field. Changing value may cause entering stand-by / software reset.

Register Value Conventions

Expression	Description
x	Undefined bit
X	Undefined multiple bits
?	Undefined, but depends on the device or pin status
Device dependent	The value depends on the device
Pin value	The value depends on the pin status

Reset Value Conventions

Expression	Description
0	Clears the register field
1	Sets the register field
x	Don't care condition

Warning: Some bits of control registers are driven by hardware or write operation only. As a result the indicated reset value and the read value after reset might be different.

1 Product Overview

This chapter includes the following sections:

- Introduction
- Features

1.1 Introduction

S5K3L6XX is a highly integrated 13M pixel camera chip that includes a CMOS image sensor (CIS), image correction functionality and serial transmission using 4-lane MIPI. It is fabricated using SAMSUNG CMOS image sensor process developed for imaging applications to realize a high-efficiency and low-power photo sensor. The sensor consists of 4208 × 3120 effective pixels (4224 × 3136 active pixels) that matches the 1/3-inch optical format.

The CIS has on-chip 10-bit ADC arrays to digitize the pixel output and on-chip Correlated Double Sampling (CDS) to reduce Fixed Pattern Noise (FPN) drastically. It incorporates on-chip camera functions such as data binning, data formatting.

S5K3L6XX is suitable for low power camera module with 2.8 V/1.05 V power supply.

1.2 Features

- 13Mp sensor with 1/3" optics
- Unit Pixel Size : 1.12 μm × 1.12 μm
- Effective Resolution : 4208 (H) × 3120 (V) pixels
- Active Resolution : 4224 (H) × 3136 (V) pixels
- Color Filter : RGB Bayer Pattern
- Shutter Type : Electronic Rolling Shutter and global reset
- Max. Normal Frame Rate : 30 fps @ Full
- Max. Video Frame Rate : 60 fps @ FHD, 120fps @ HD
- Data rate : 1.25 Gbps/lane
- ADC Accuracy : 10 bits
- Interfaces :
  - MIPI CSI-2 (1.25 Gbps per lane, 4 lanes)
  - Output formats - RAW8 (truncated), RAW10
- Control interface : I2C-compatible / 2'nd I2C Slave address support for Dual camera
- 3.5 Kbits of On-chip OTP memory for users
- Analog gain x16
- Vertical Flip and Horizontal Mirror mode
- Average-sub-sampling - 2/2
- Bad Pixel Correction
- Built-in test pattern generation
- Supply voltage : 2.8 V for analog, 1.8 V or 2.8 V for I/O, and 1.05 V for digital core supply
- Operating temperature : –30 °C to + 70 °C
- Backside illumination(BSI) structure

2 Pad Configuration

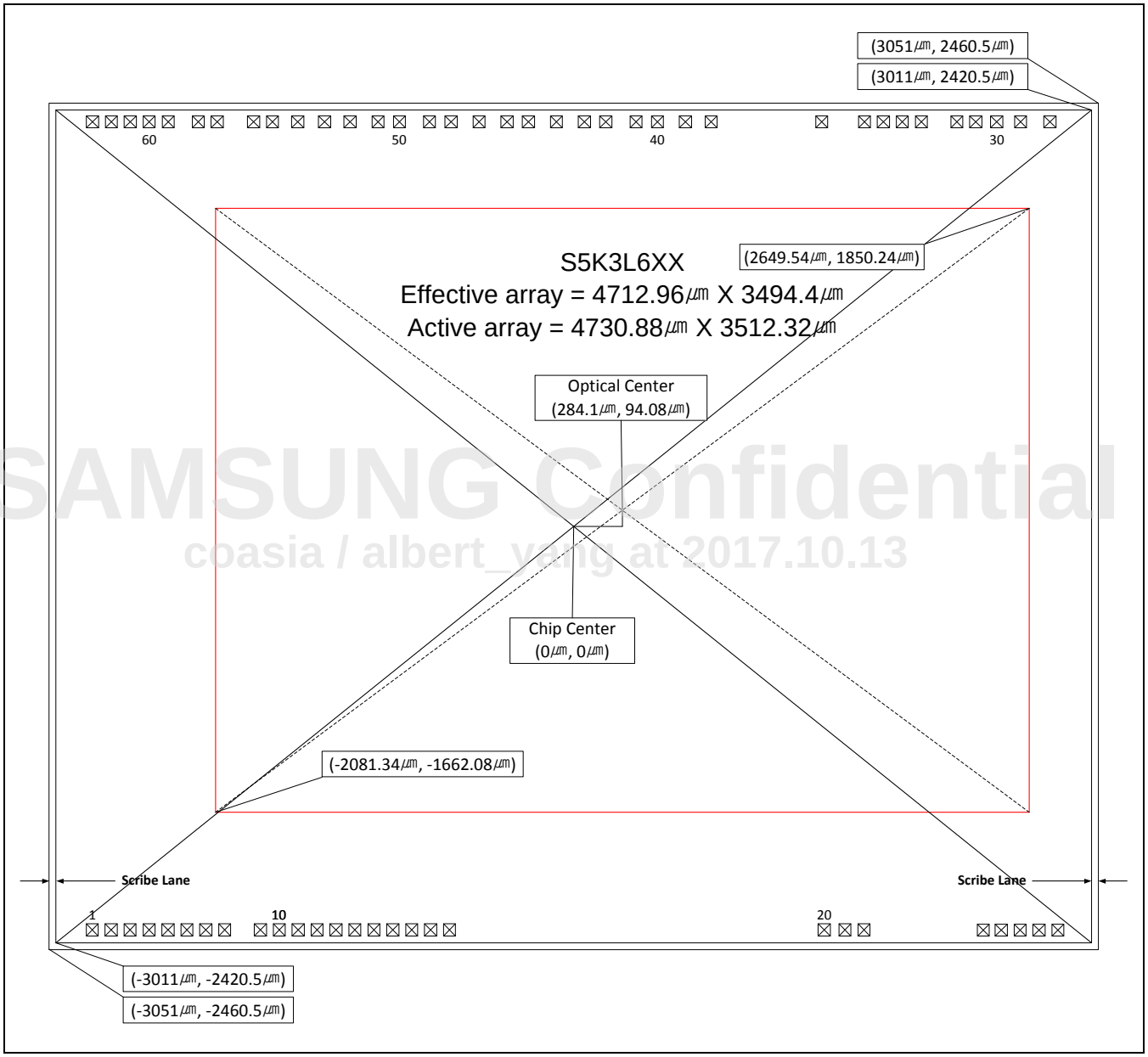


Figure 1 Top View of Chip Dimension

2.1 Pad Description

Table 1 Pad Description

Pad No.	Pad Name	Type	A/D	Description
1	VSSD	GND	D	Digital Ground
2	VDDD	PWR	D	Digital Power(1.05V)
3	VDDA	PWR	A	Analog Power(2.8V)
4	VSSA	GND	A	Analog Ground
5	VDDA	PWR	A	Analog Power(2.8V)
6	VSSA	GND	A	Analog Ground
7	VDDD	PWR	D	Digital Power(1.05V)
8	VSSD	GND	D	Digital Ground
9	XSHUTDOWN	I	D	Master Reset. Active low (XSHUTDOWN)
10	SCK	I	D	IIC Slave Clock. It must be connected to 2.2kΩ pull-up resistor.
11	SDI	BI	D	IIC Slave Data. It must be connected to 2.2kΩ pull-up resistor.
12	VSYNC_OUT	BI	D	Vertical SYNC out
13	TST	I	D	Mode define (0: default Normal)
14	NC	NC	NC	NC
15	NC	NC	NC	NC
16	VSYNC_IN	BI	D	Vertical SYNC in
17	NC	NC	NC	NC
18	VDDIO	PWR	D	IO Power (1.8V)
19	VSSIO	GND	D	IO Ground
20	NC	NC	NC	NC
21	VDDD	PWR	D	Digital Power(1.05V)
22	VSSD	GND	D	Digital Ground
23	NC	NC	NC	NC
24	VSSA	GND	A	Analog Ground
25	VDDA	PWR	A	Analog Power(2.8V)
26	VSSA	GND	A	Analog Ground
27	VDDA	PWR	A	Analog Power(2.8V)
28	VNTG	BI	A	VNTG
29	VRGSL	BI	A	VRGSL
30	NC	NC	NC	NC
31	VDDA	PWR	A	Analog Power(2.8V)
32	VSSA	GND	A	Analog Ground
33	VSSA	GND	A	Analog Ground

Pad No.	Pad Name	Type	A/D	Description
34	VDDA	PWR	A	Analog Power(2.8V)
35	VSSD	GND	D	Digital Ground
36	VDDD	PWR	D	Digital Power(1.05V)
37	VDDA_M	PWR	A	MIPI Analog Power(2.8V)
38	VDDD_M	PWR	D	MIPI Digital Power(1.05V)
39	VSSD_M	GND	D	MIPI Digital Ground
40	M_DN0	O	D	MIPI data lane 0 negative
41	M_DP0	O	D	MIPI data lane 0 positive
42	M_DN1	O	D	MIPI data lane 1 negative
43	M_DP1	O	D	MIPI data lane 1 positive
44	NC	NC	NC	NC
45	M_CLKN	O	D	MIPI clock lane negative
46	M_CLKP	O	D	MIPI clock lane positive
47	NC	NC	NC	NC
48	M_DN2	O	D	MIPI data lane 2 negative
49	M_DP2	O	D	MIPI data lane 2 positive
50	M_DN3	O	D	MIPI data lane 3 negative
51	M_DP3	O	D	MIPI data lane 3 positive
52	VSSD_M	GND	D	MIPI Digital Ground
53	VDDD_M	PWR	D	MIPI Digital Power(1.05V)
54	VDDA_M	PWR	A	MIPI Analog Power(2.8V)
55	NC	NC	NC	NC
56	NC	NC	NC	NC
57	VDDIO	PWR	D	IO Power (1.8V)
58	VSSIO	GND	D	IO Ground
59	EXTCLK	I	D	External clock from 6MHz to 32MHz
60	VDDD	PWR	D	Digital Power(1.05V)
61	VSSD	GND	D	Digital Ground
62	VDDD	PWR	D	Digital Power(1.05V)
63	VSSD	GND	D	Digital Ground

2.2 Application Circuit

Figure 2 illustrates the top view of a module application circuit.

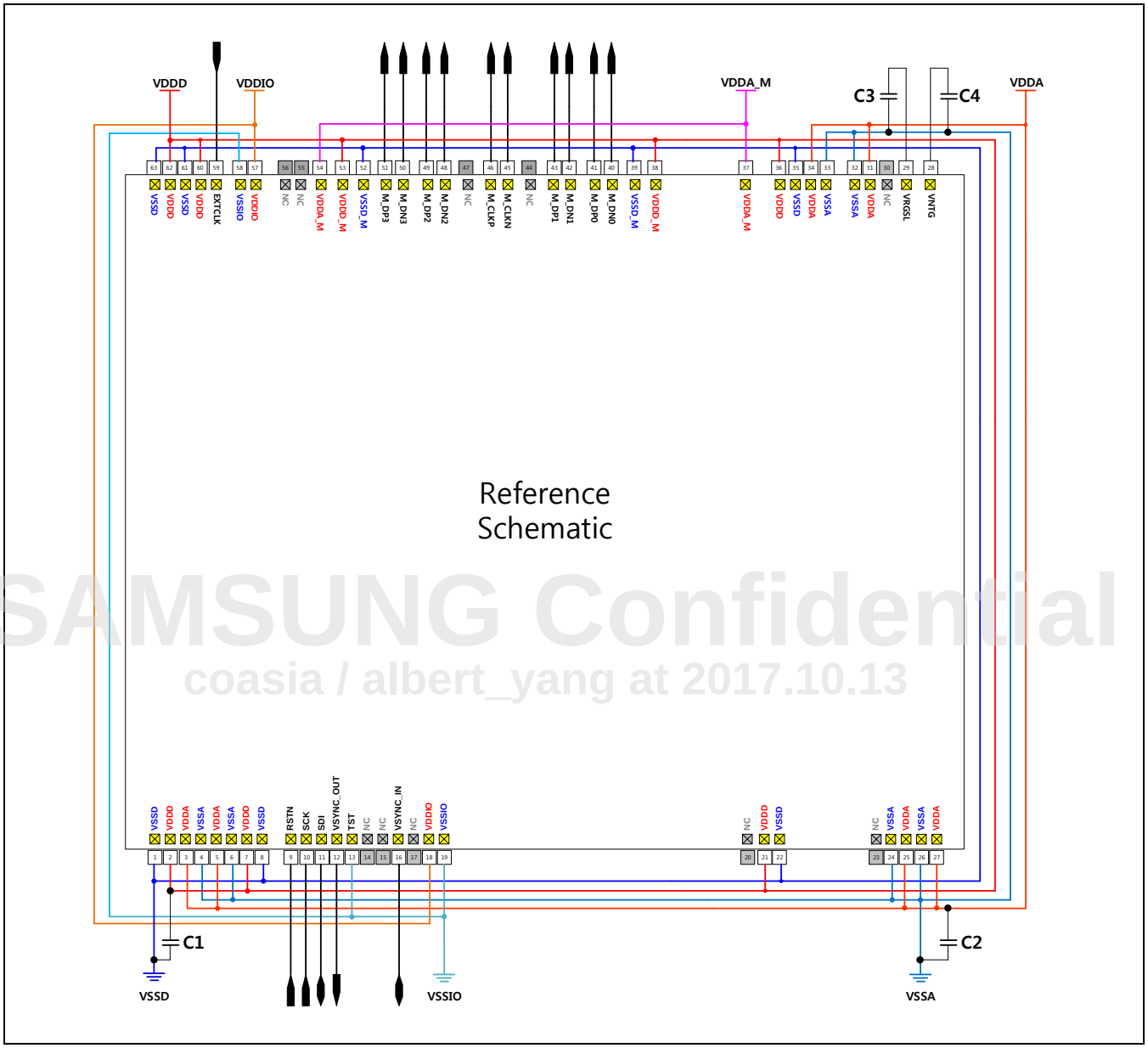


Figure 2 Top View of Module Application Circuit

2.3 Pixel Array Information

Figure 3 illustrates the top view of pixel array information.

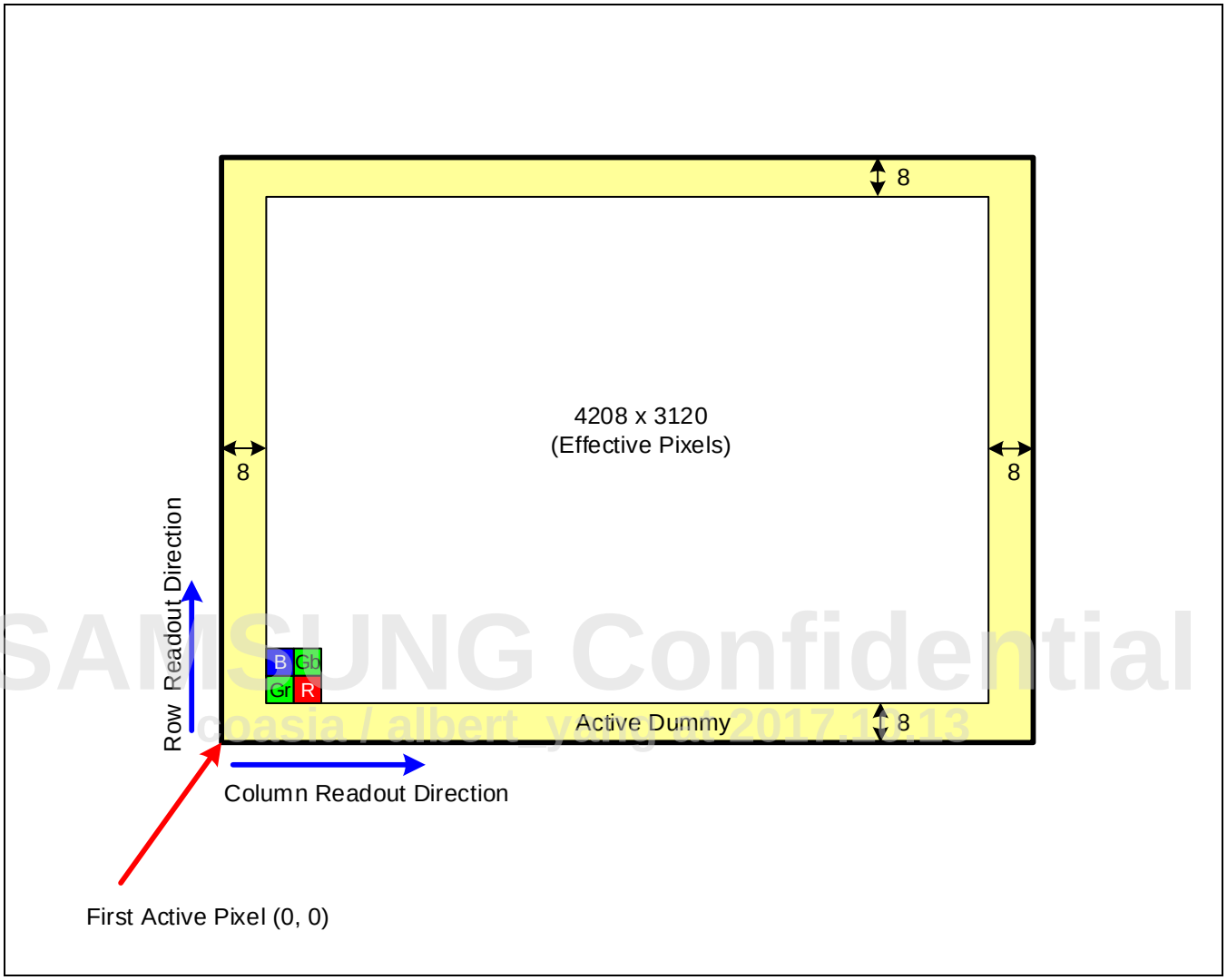


Figure 3 Top View of Pixel Array Information

3 Power Sequence

3.1 Operating Modes

Sensor module has four operating modes such as power-off, hardware standby, software standby and streaming (*Table 2*). Transition from one mode to another is achieved by issuing the appropriate mode command via the CCI serial control interface, the RSTN (XSHUTDOWN) signal changing state and the power supplies. By default, S5K3L6XX powers up with the CSI-2 serial data interface enabled. *Figure 4* illustrates the valid mode changes for the sensor module.

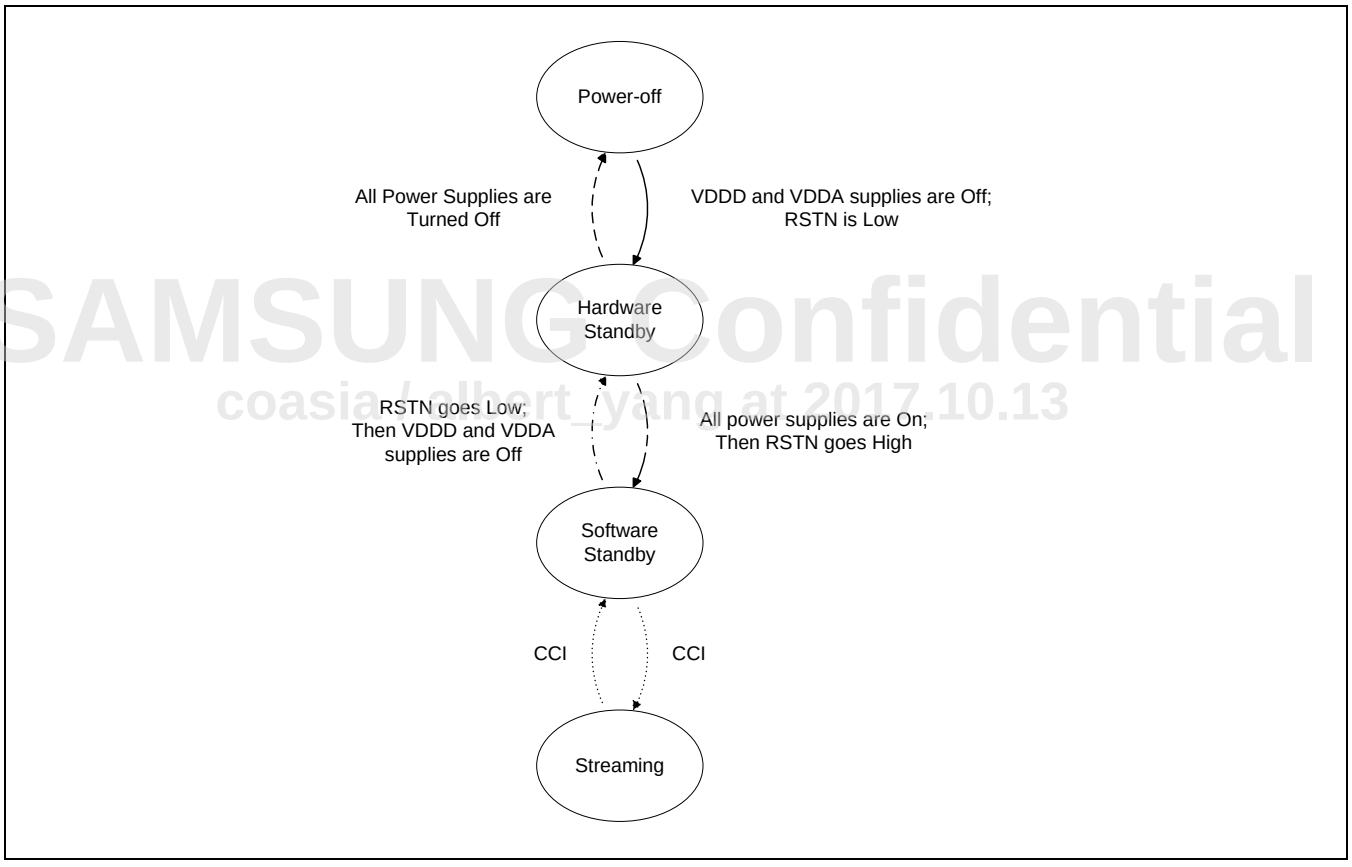


Figure 4 System State Diagram

Table 2 Operating Mode Summary

Power State	Description
Power-off	Power supplies are turned off.
Hardware standby	No communication with the sensor is possible. Internal core power shut-off only by external VDDD power down.
Software standby	CCI communication with sensor is possible. Core power is on.
Streaming	The sensor module is fully powered and is streaming image data on the CSI-2 bus.

Table 3 describes the registers that control the operating mode of the camera module

Table 3 Operating Mode Registers

Name	Bit	Width	Description	Start	Reset Value
mode_select	[0:0]	RW	0 = Software Standby 1 = Streaming	0x0100	0x00

3.2 Power-Up Sequence

The digital and analog supply voltages are powered up in any order, for example, VDDD/VDDIO then VDDA or VDDA/VDDIO then VDDD.

After power up, RSTN (XSHUTDOWN) should be low when the power supplies are brought up, then the sensor module will go into hardware standby mode. As long as RSTN is low and VDDD is down, the sensor module stays in hardware standby mode.

The assertion of RSTN ensures that the CCI register values are initialized correctly to their default values.

When RSTN will go 'high', all PADs will exit from FAIL-SAFE mode, and switch to Normal operating mode.

The MCLK clock can either be initially low and then enabled during software standby mode or MCLK can be a free running clock.

Table 4 Power-Up Sequence Timing Constraints

Constant	Label	Min.	Max.	Unit
VDDD / VDDA / VDDIO rising time	t0	VDDIO, VDDA and VDDD may rise in any order. The rising separation time can vary from 0 ns to indefinite		ns
VDDD rising to RSTN (XSHUTDOWN) rising	t1	0.0	–	ns
RSTN (XSHUTDOWN) rising to first CCI transaction	t2	10	–	us
Minimum no. of MCLK cycles prior to the first CCI transaction	t3	23,000	–	MCLK cycles
PLL start up lock time	t4	–	1	ms
Entering streaming mode – First frame start sequence (fixed part)	t5	–	10	ms
Entering streaming mode – First frame start sequence (variable part)	t6	The delay is the coarse integration time value		lines
DPHY initialization period (TINIT)	t7	0.1	–	ms

NOTE:

1. At hardware standby mode external VDDD should be OFF.
2. For minimal SW standby power external clock (MCLK) should be off
3. S5K3L6XX does not support power gating in stand-by mode. For minimal power consumption it is necessary to power down externally in standby mode.

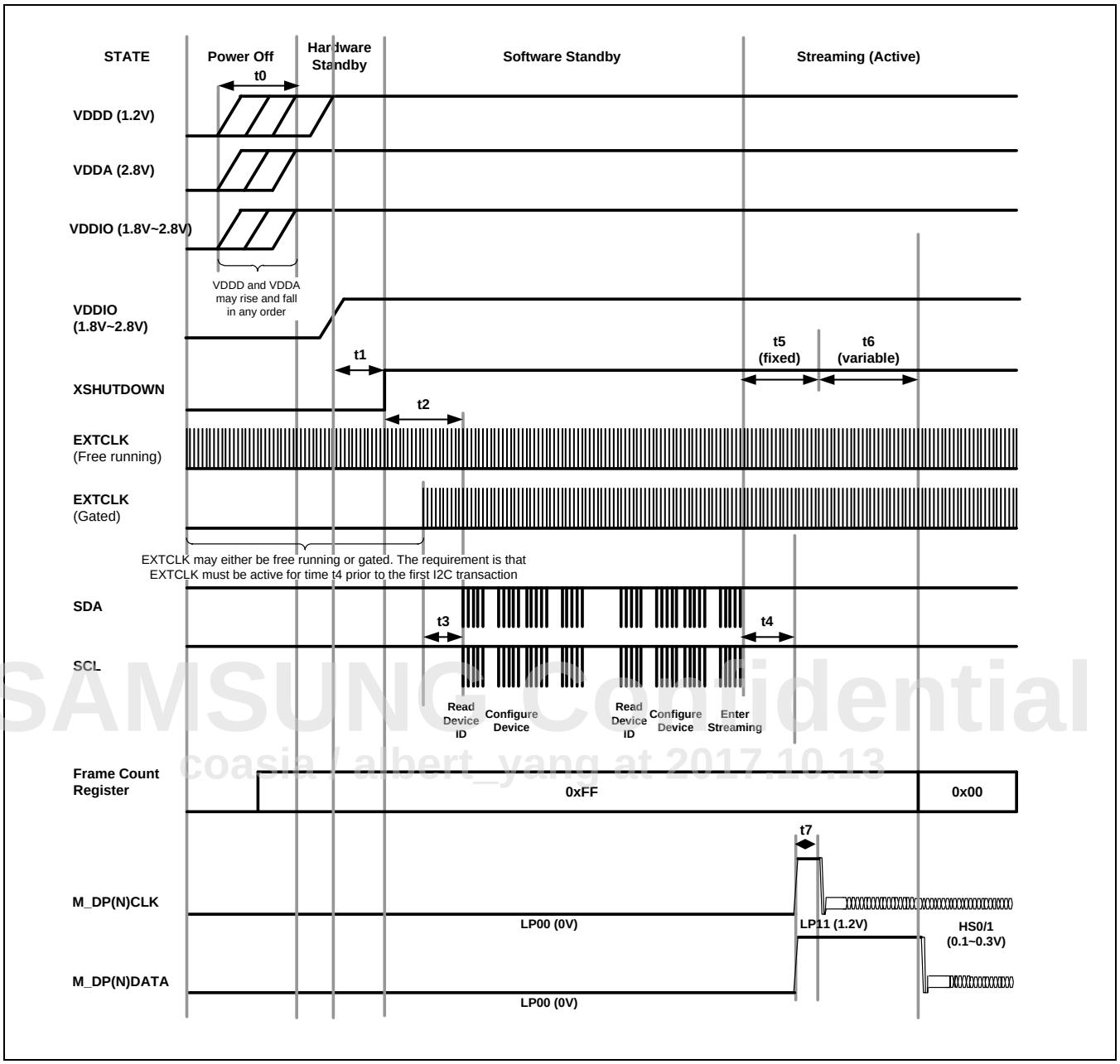


Figure 5 Power-Up Sequence

3.3 Power-Down Sequence

The digital and analog supply voltages can be powered down in any order, for example VDDD/VDDIO then VDDA or VDDA/VDDIO then VDDD.

Similar to the power-up sequence, the MCLK : input clock is either gated or continuous.

If the CCI command to exit streaming is received when a frame of valid active data is being output, then the sensor module must wait for the frame end code before entering the software standby mode. Frame end code may come either after all frame pixels were transmitted or during the frame when next line transmission is completed - based on a configuration register (Refer to S5K3L6XX application notes for details)

If the CCI command to exit streaming mode is received during the inter frame time, then the sensor module must immediately enter the software standby mode.

Table 5 Power Down Sequence Timing Constraints

Constant	Label	Min.	Max.	Unit
Enter software standby CCI command-device in software standby mode	t0	When MIPI frame is sent as output, the data waits for the MIPI frame end code before entering software standby mode; For other cases, data immediately enters software standby mode.		–
Minimum number of MCLK cycles after the last CCI transaction or MIPI frame end code.	t1	512	–	MCLK cycles
Last CCI Transaction or MIPI frame end code-RSTN (XSHUTDOWN) falling	t2	512	–	
RSTN (XSHUTDOWN) falling to VDDD falling	t3	0.0	RSTN falling and VDDD falling can be in any order	ns
VDDD falling to RSTN (XSHUTDOWN) falling	t4	0.0		
VDDA/VDDD/VDDIO falling time	t5	VDDA/VDDD/VDDIO can fall in any order. The rising separation varies from 0 ns to indefinite		

NOTE: For minimal power during hardware standby mode external VDDD should be tuned off.

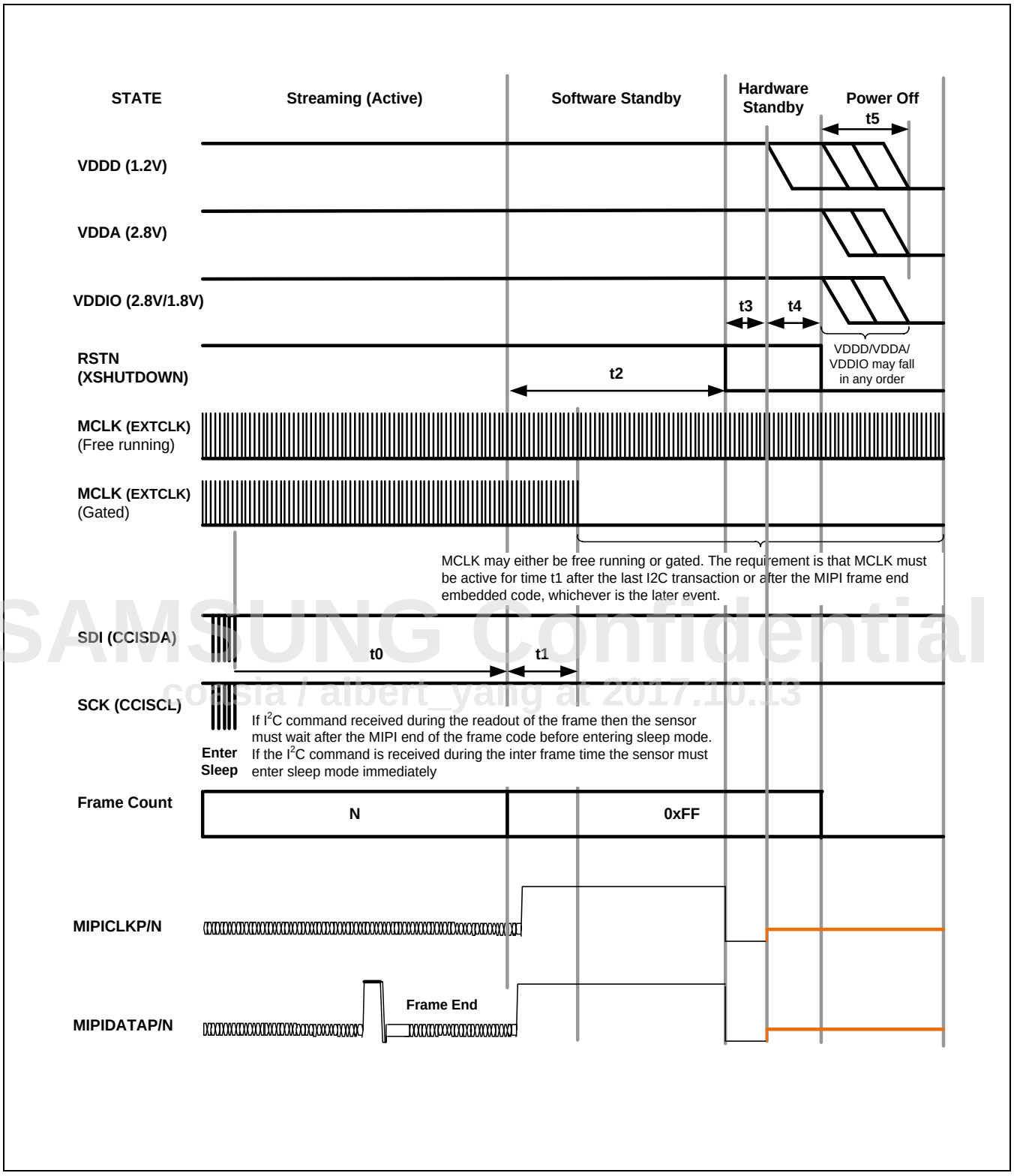


Figure 6 Power-Down Sequence

4 Control Interface

4.1 Camera Control Interface (CCI)

S5K3L6XX supports the Camera Control Interface (CCI), an I2C fast-mode compatible interface, to control the transmitter. S5K3L6XX always acts as a slave in the CCI bus. CCI is capable of handling several slaves in the bus, but multi-master mode is not supported. Typically only receiver and transmitter are connected to the CCI bus. This ensures a pure S/W implementation.

CCI is different from the system I2C bus, however I2C compatibility ensures that it is also possible to connect the transmitter to the system I2C bus. CCI is a subset of I2C protocol including the minimum combination of obligatory features for I2C slave device specified in the I2C specification. Therefore transmitters complying with the CCI specification can also be connected to system I2C bus. However, it is important to ensure that the I2C masters do not try to utilize those I2C features, which are not supported in transmitters complying with the CCI specification. Each transmitter conformed to the CCI specification has additional features implemented to support I2C.

4.1.1 Data Transfer Protocol

The data protocol is according to I2C standard specified in I2C specification.

4.1.2 Message Format

S5K3L6XX CCI supports 16-bit index with 8-bit data with basic I2C standard protocol; START condition, slave address with read/write bit, acknowledge from slave, and STOP condition. In read operation, data byte comes from slave till negative ack is asserted from master. The default device address for the sensor is 0010000b and TAT PAD changes it. Table 7 describes the defined address settings.

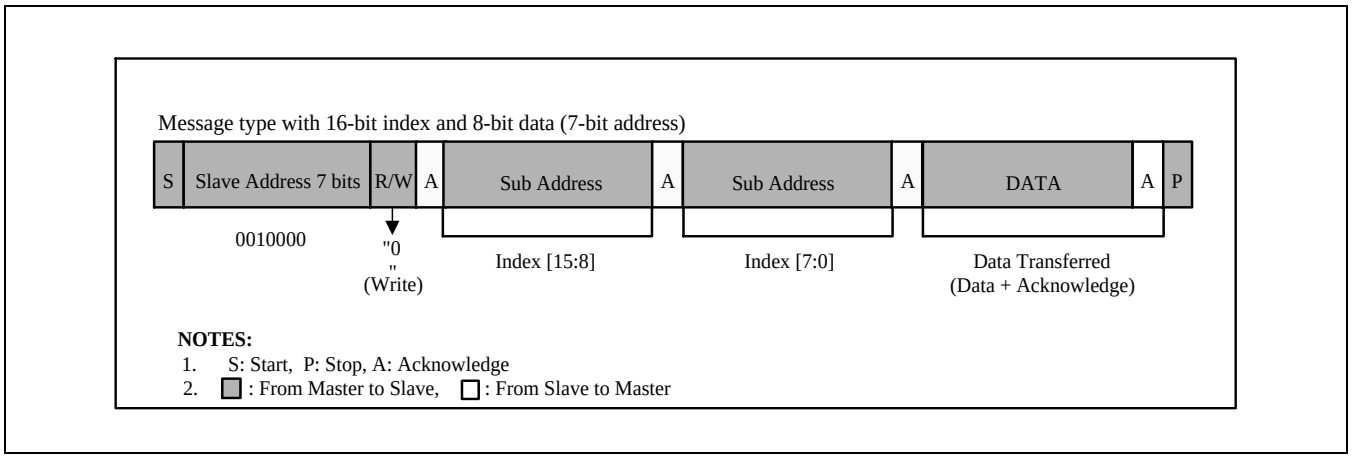
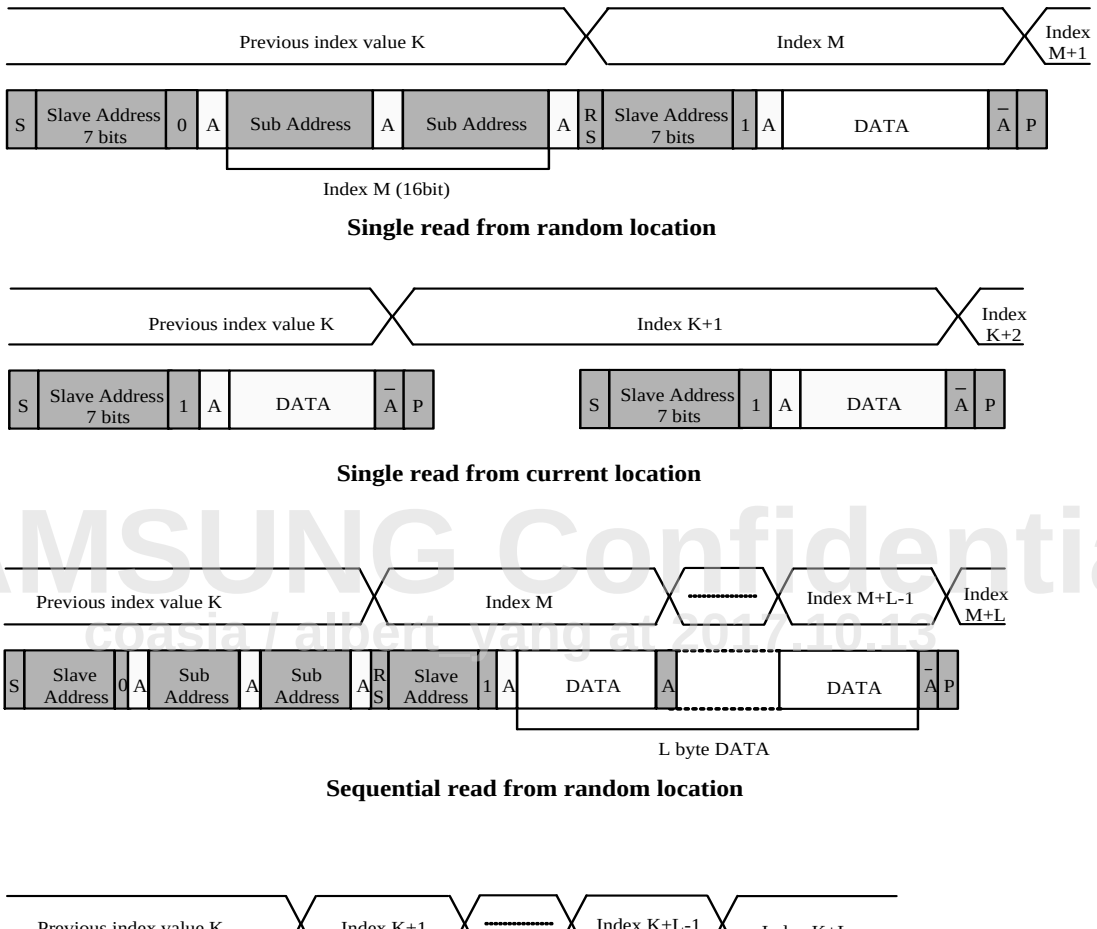


Figure 7 CCI Message Type

4.1.3 Read/Write Operation

S5K3L6XX CCI interface must support four different read operations and two different write operations such as single read from random location, sequential read from random location, single read from current location, sequential read from current location, single write to random location, and sequential write starting from random location. The read/write operations are illustrated in Figure 8. The 16-bit index in the slave device has to be auto incremented after each read/write operation.



NOTES:
1. S: Start, P: Stop, RS: Restart
   A: Acknowledge, A: Negative acknowledge,
2. ■ : From Master to Slave, □ : From Slave to Master

Figure 8 CCI Read Operation

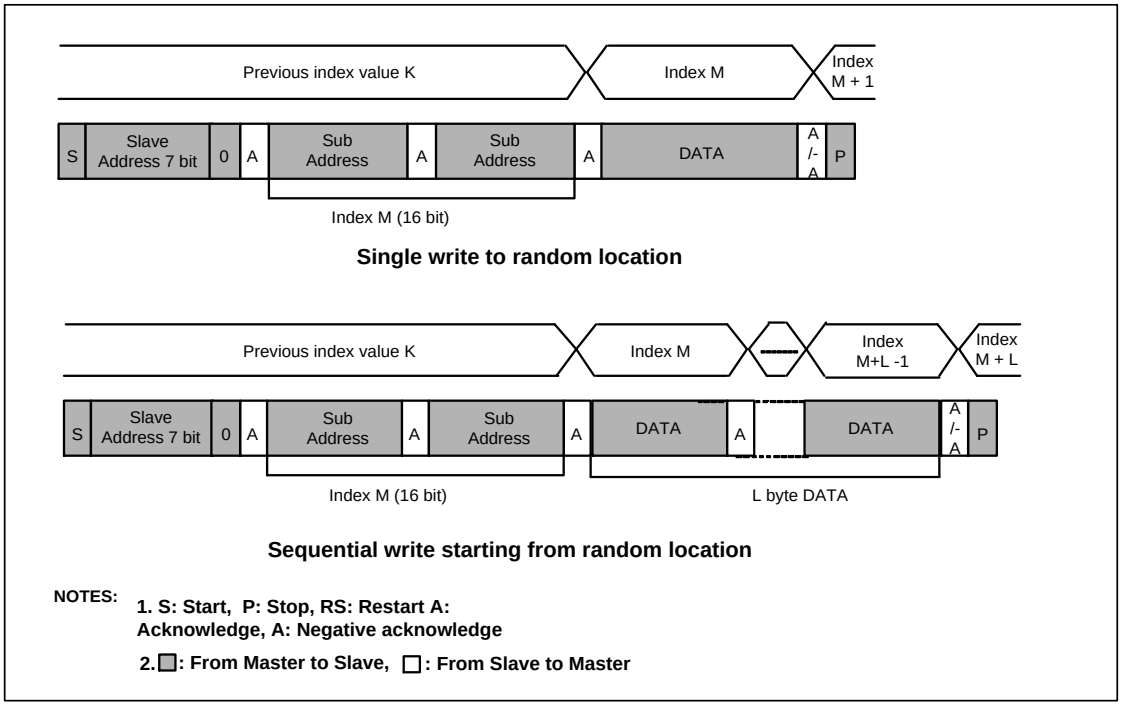


Figure 9 CCI Write Operation

4.2 CCI Timing

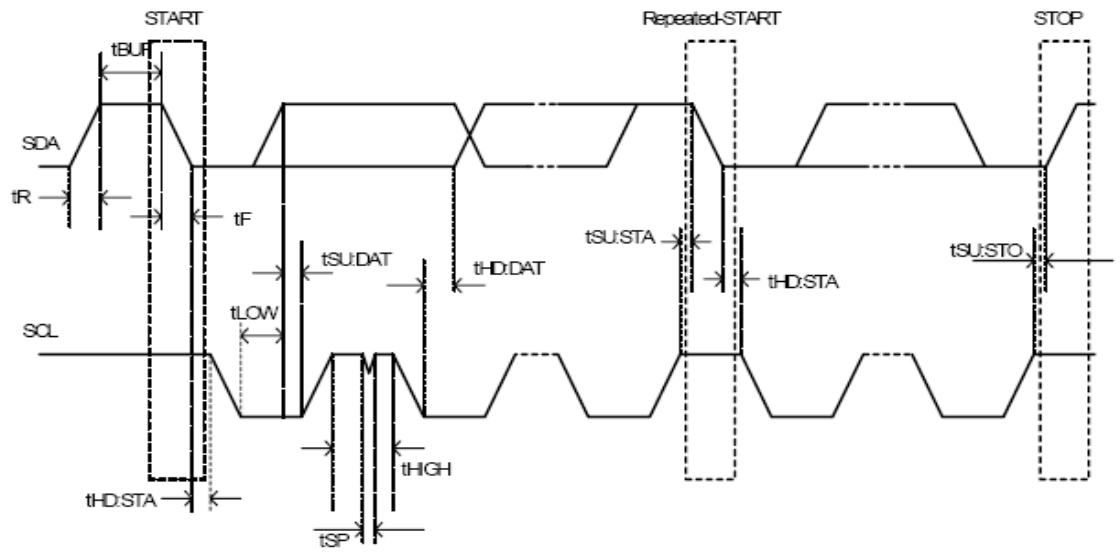


Figure 10 CCI Timing

Table 6 CCI Timing Specifications

(V_{IHmin} = 0.9 V_{DD}, V_{ILmax} = 0.1 V_{DD}, External pull-up resister = 4.7 kΩ at SCL/SDA for Fast-mode)

Parameter	Symbol	Standard-Mode		Fast-Mode		Unit
		Min.	Max.	Min.	Max.	
Output fall time from VIHmin to VILmax	tof	–	250	20 + 0.1 CB (NOTE)	250	ns
Pulse width of spikes which must be suppressed by the input filter.	tSP	N/A	N/A	0	50	ns
SCL clock frequency	fSCL	0	100	0	400	kHz
Hold time (repeated) start condition. After this period, the first clock pulse is generated	tHD:STA	0.4	–	0.6 (6)	–	µs
Low period of the SCL clock	tLOW	4.7	–	1.3	–	µs
High period of the SCL clock	tHIGH	4.0	–	0.6 (5)	–	µs
Setup time for a repeated start condition	tSU:STA	4.7	–	0.6	–	µs
Data hold time	tHD:DAT	0 (3)	3.45 (4)	0 (3)	0.9 (4)	µs
Data setup time	tSU:DAT	250 (2)	–	100 (2)	–	ns
Rise time of both SDA and SCL signals	tr	–	1000	20 + 0.1 CB (NOTE)	300	ns
Fall time of both SDA and SCL signals	tf	–	300	20 + 0.1 CB (NOTE)	300	ns
Setup time for stop condition	tSU:STO	4.0	–	0.6	–	µs
Bus free time between a stop and start condition	tBUF	4.7	–	1.3	–	µs

NOTE: CB: from 10 pF to 400 pF

1. CB = Total capacitance of one bus line in pF
2. A aast-mode I2C-bus device is used in a standard-mode I2C-bus system, but the requirement tSU:DAT ≥ 250 ns must be then met. This is done automatically if the device does not stretch the Low period of the SCL signal. If such device does stretch the low period of SCL signal, it must output the next data bit to the SDA line trMAX + tSU:DAT = 1000 + 250 = 1250 ns (according to the standard-mode I2 bus specification) before the SCL line is released.
3. A device must internally provide a hold time of at least the half period of pixel clock for the SDA signal (referred to the VIHmin of the SCL signal) to bridge the undefined region of the falling edge of SCL.
4. The maximum tHD:DAT has only to be met if the device does not meet the low period (tLOW)of the SCL signal.
5. 0.6 µs is available with the external clock 14 MHz over range.
6. For S5K3L6XX, the minimum value of tHD:STA needs one more condition: that is min. tHD:STA > Pixel clock period.

4.3 CCI Slave ID

It is possible to configure up to two CCI slave addresses using TST pin.

Table 7 CCI Slave ID Address (TST Pad)

TST	Slave Address (7-bit + Read Mode)	Slave Address (7-bit + Write Mode)	Comment
0	0010_0001b/21h	0010_0000b/20h	Address 1
1	0101_1011b/5Bh	0101_1010b/5Ah	Address 2

5 Functional Features

5.1 Block Diagram

S5K3L6XX is a progressive-scan sensor that generates a stream of pixel data at a constant frame rate. It uses an on-chip, Phase-Locked Loop (PLL) to generate all internal clocks from a single master input clock running between 6MHz and 32 MHz. Dedicated PLL generates the output interface clocks for maximum flexibility in interface frequency and to avoid EMI. The maximum pixel rate is 1.25 Gbps at MIPI 4-lane, corresponding to the pixel rate of 120 MHz at CSI-2 RAW10.

The block diagram of the sensor is illustrated in *Figure 11*.

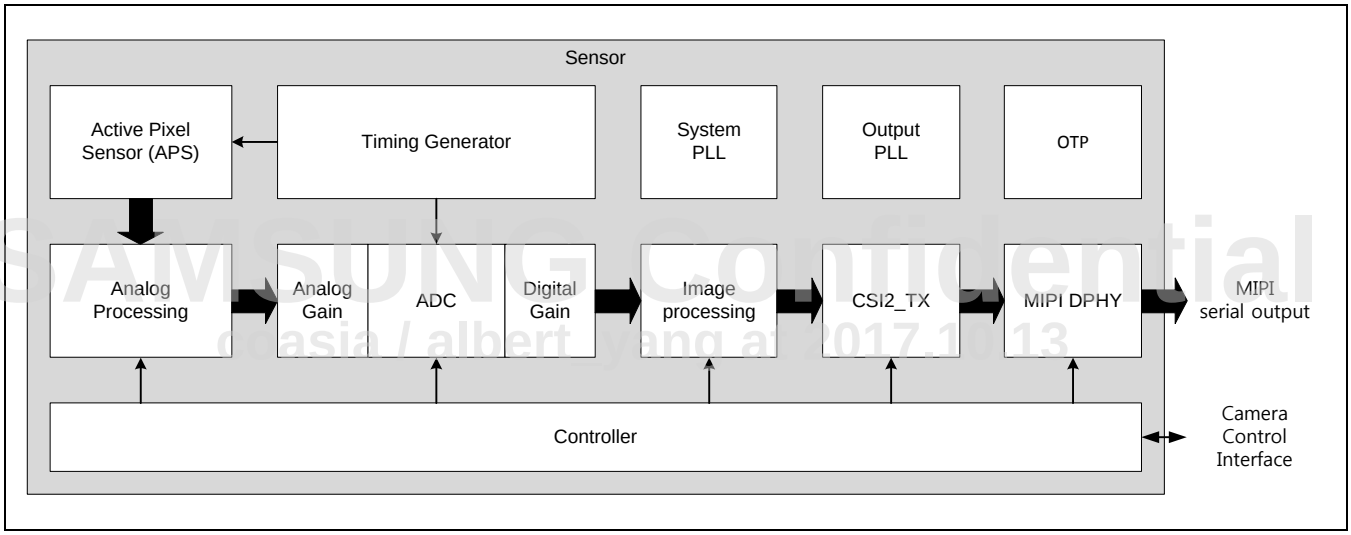


Figure 11 Function Block Diagram

The image sensor has an on-chip ADC. Column parallel ADC scheme is used for low power analog processing.

The analog output signal of each pixel includes some temporal random noise caused by the pixel reset action and some fixed pattern noise caused by the in-pixel amplifier offset deviation. To eliminate those noise components, a Correlated Double Sampling (CDS) circuit is used before converting to digital.

The output from the ADC is a 10-bit value for each pixel in the array. The ADC output passes through a digital processing signal chain which provides further data path corrections and applies digital gain. A shading correction block is used to compensate for color/brightness shading introduced by the lens. It has additional functionalities such as deterministic pattern generator, and a MIPI CSI-2 frame formatter with embedded line support.

5.2 Pixel Array Addresses

Addressable pixel array is defined as the pixel address range to be read. The Addressable pixel array can be assigned anywhere on the pixel array. x_addr_start, y_addr_start, x_addr_end and y_addr_end register control the addressed region of the pixel array.

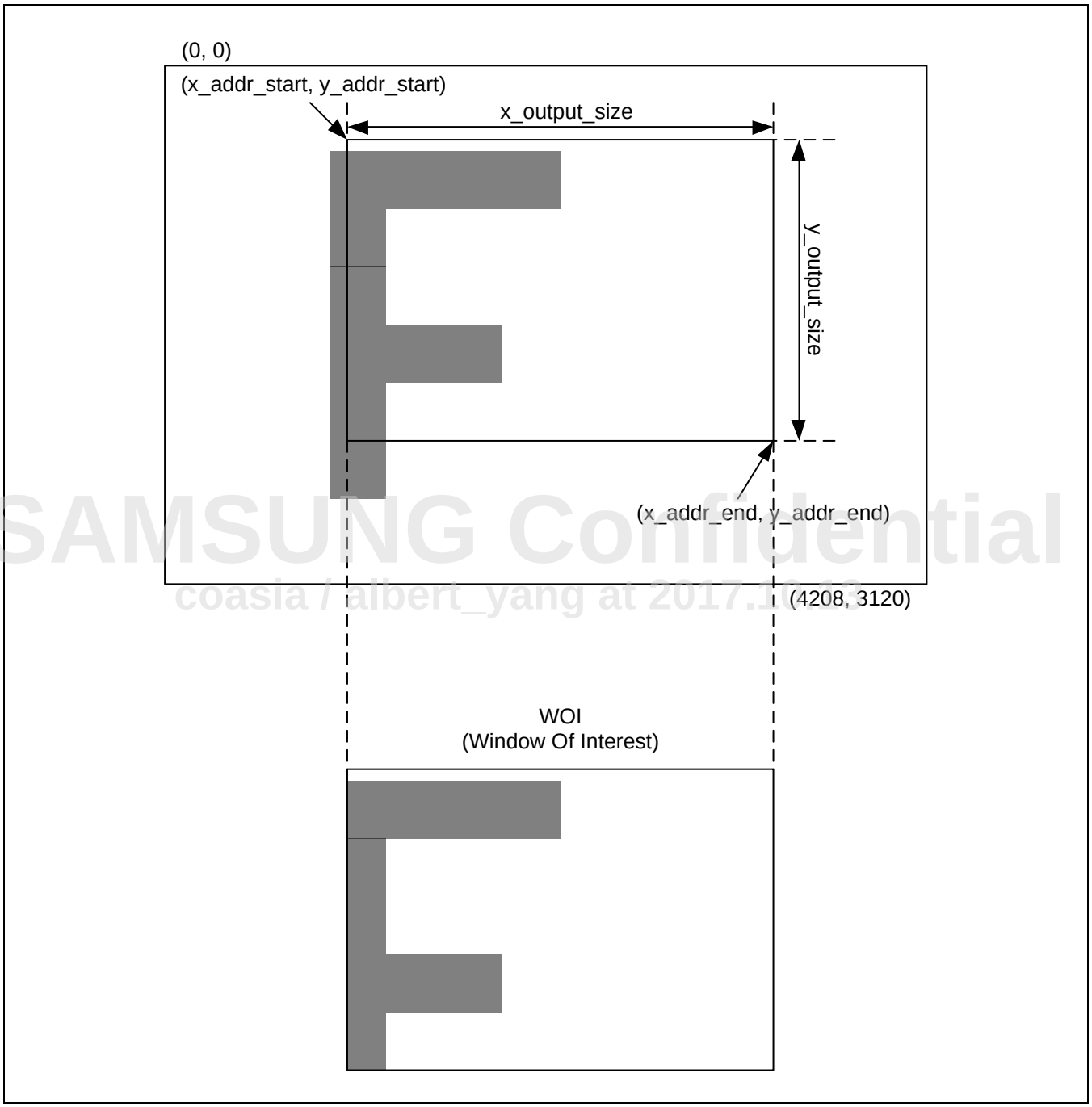


Figure 12 Window of Interest on Pixel Array

5.3 Horizontal Mirror and Vertical Flip

The pixel data is normally read out from left to right in the horizontal direction and from top to bottom in the vertical direction. By changing the mirror/flip mode, the read-out sequence can be reversed, and the resulting image can be flipped like a mirror image. Pixel data is then read out from right to left in horizontal mirror mode and from bottom to top in vertical flip mode. Image orientation register programs the horizontal mirror and vertical flip mode.

The sensor module supports four possible pixel readout orders according to the directions of pixel readout and line readout: standard readout, horizontally mirrored readout, vertically mirrored readout, horizontally mirrored and vertically flipped readout.

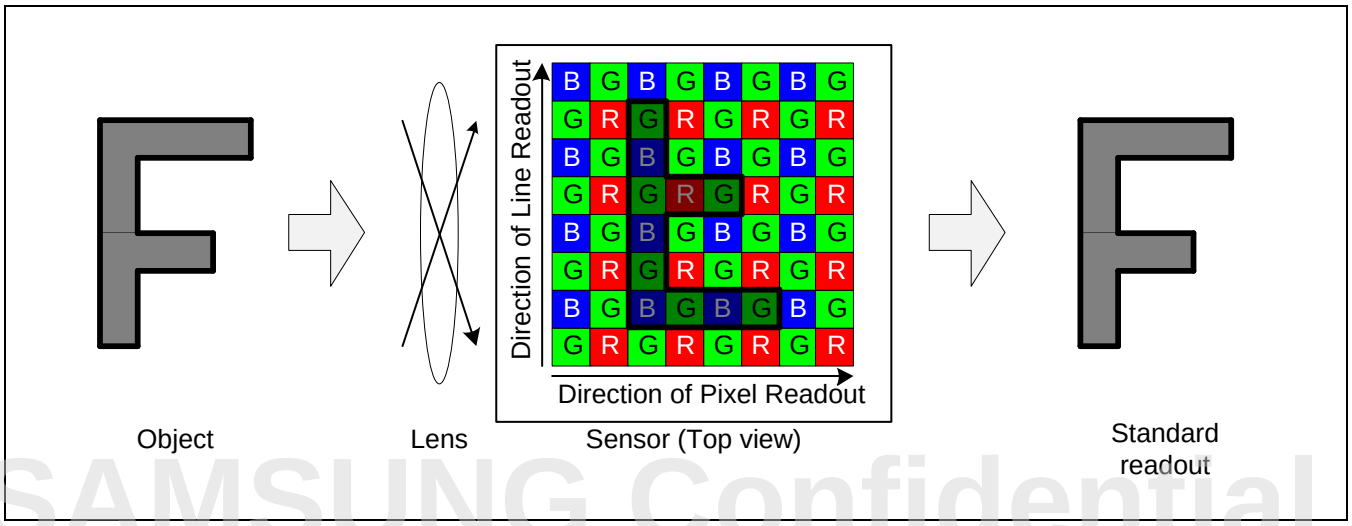


Figure 13 Object, Sensor and Displayed Image in Standard Readout

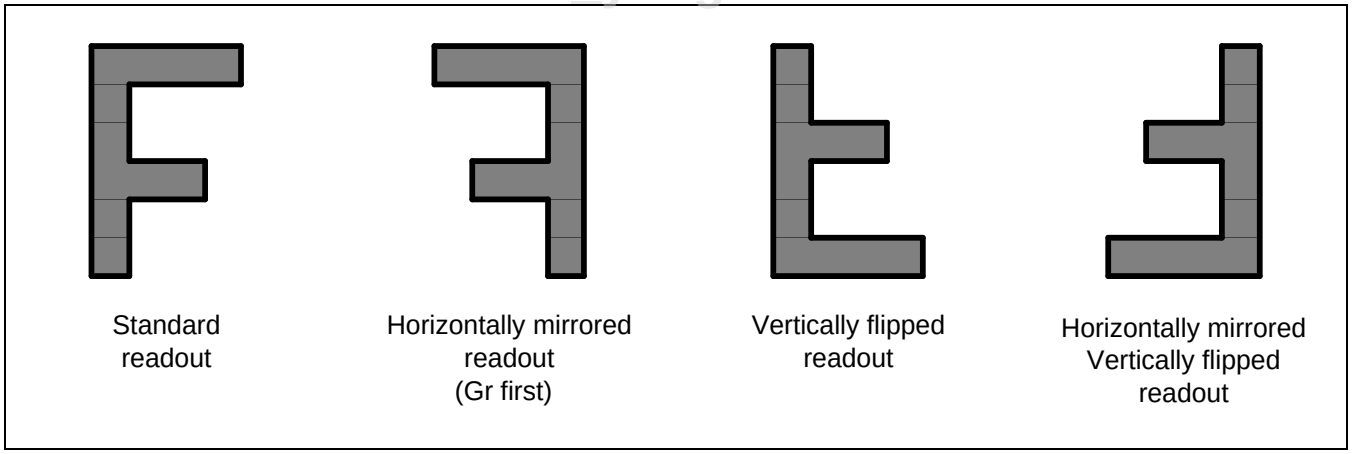


Figure 14 Four Readout Orders and Displayed Images

5.4 Averaged Sub-Sampled Readout

Averaged sub-sampled readout (binning readout) is available. By programming the averaged sub-sampling enable register, the sensor can be configured to read out pixel data that has been averaged with adjacent pixels.

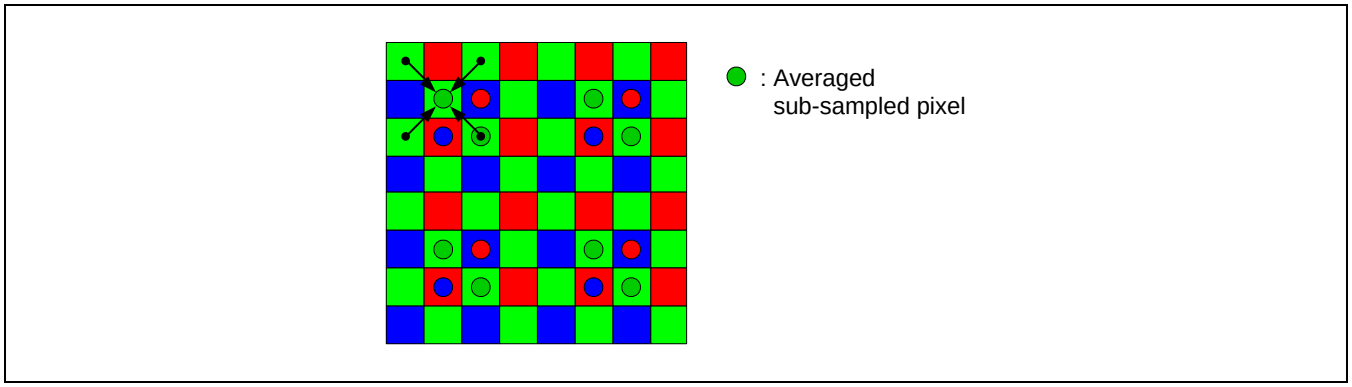


Figure 15 Example of 2 by 2 Averaged sub-Sampled Readout

5.5 Frame Rate Control

Varying the frame size changes the line rate and the frame rate. line_length_pck and frame_length_lines registers control the width and depth of the virtual frame. The horizontal and vertical blanking times (horizontal blanking time: line_length_pck-x_output_size, vertical blanking time: frame_length_lines-y_output_size) should meet the system requirements. Use the following formula to calculate the frame rate :

Frame rate = vt_pix_clk/(frame_length_lines × line_length_pck)

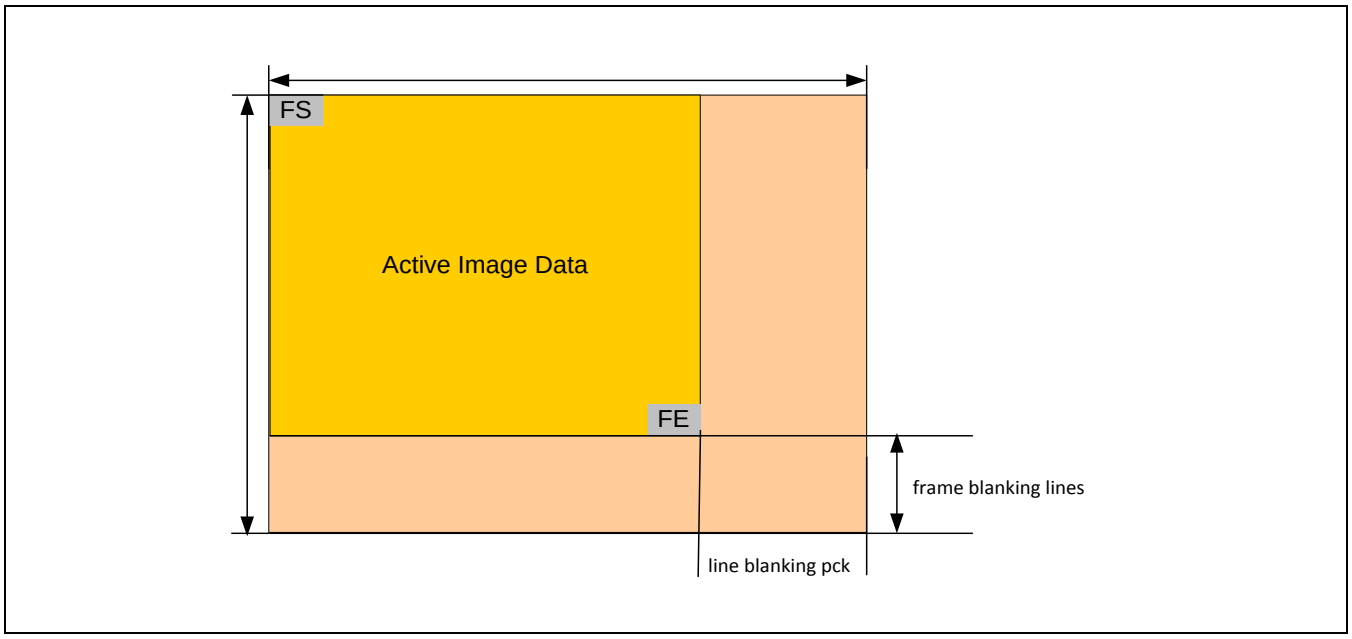


Figure 16 Virtual Frame Format Example

5.5.1 Integration Time Control (Electronic Shutter Control)

The shutter operation controls the pixel integration time. During the shutter operation, the column Step Integration Time Control Register (fine_integration_time) and the line Step Integration Time Control Register (coarse_integration_time) determine the amount of time, that is, integration time. Use the following formula to calculate the total integration time of the sensor module:

Total_integration_time = {coarse_integration_time × line_length_pck + fine_integration_time} × pclk period[sec]

5.5.2 Functional Operation Modes

S5K3L6XX supports various types of operation modes.

Operation mode is function of several mode parameters such as:

- Interface bandwidth
- Requested sensor output size and sensor operation mode
- CIS output size and number of bits per pixel e.g. RAW10, RAW8 (truncated)
- Required Vertical blank time

Typical operation modes and related typical settings are described in Table 8.

Table 8 Typical Functional Operation Modes

Mode	Frame rate	CIS Output		Binning		Image Mode
		H	V	H	V	
13 Mp	30 fps	4208	3120	1	1	Full size
FHD	60 fps	1920	1080	2	2	Binning and Crop
HD	120 fps	1280	720	2	2	Binning and Crop

5.6 PLL and Clock Generator

S5K3L6XX clock system uses system Phase-Locked Loop (PLL) and system clock dividers to generate all internal clocks from a single master input clock running between 6 MHz and 32 MHz.

Output interface clocks are generated by the dedicated Output PLL (for EMI avoidance). The maximum PLL VCO frequency is 1 GHz for SYSTEM PLL and 2.15GHz for OUTPUT PLL.

Clock dividers generate all system clocks from PLL sources.

Charge pump and ADC clocks are used for A/D conversion circuits, pixel clock is used for pixel processing and sensor control. Bit clock and output clock are set according to required output rate.

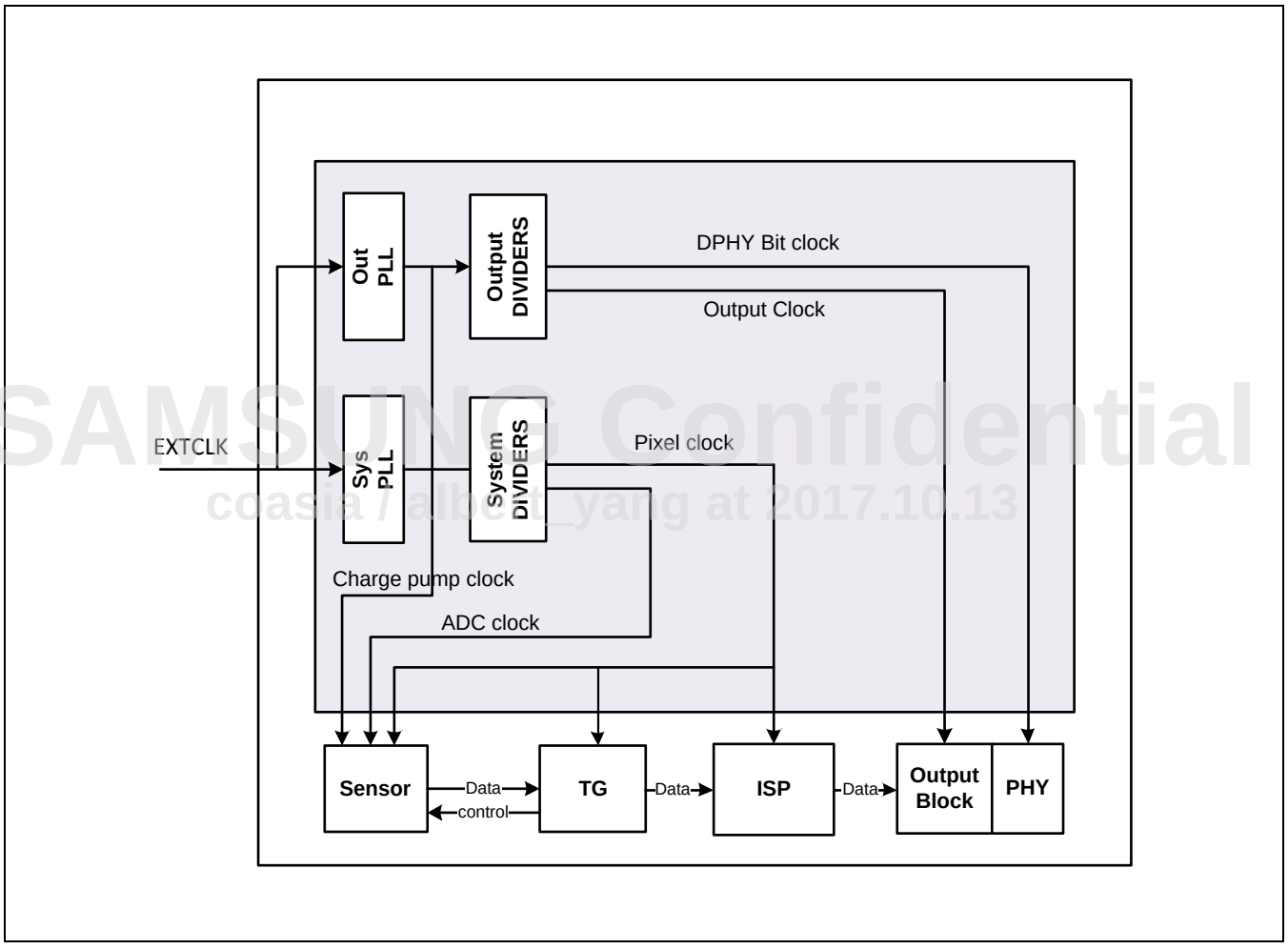


Figure 17 Block Diagram of Clock System

5.6.1 Clock Relationships

The host provides the external input clock (with values varying between 6 and 32 MHz) in addition to setting dividers and multiplier to receive the required video timing and output pixel clocks.

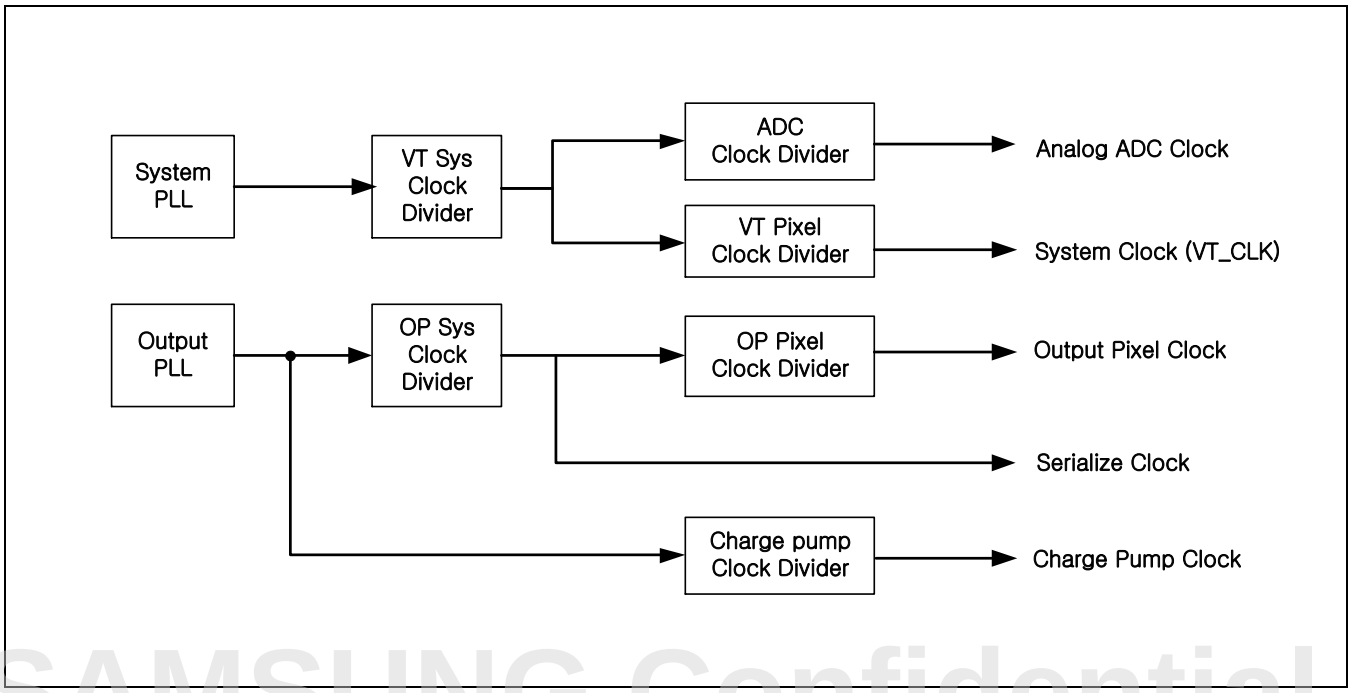


Figure 18 Clock Relationships

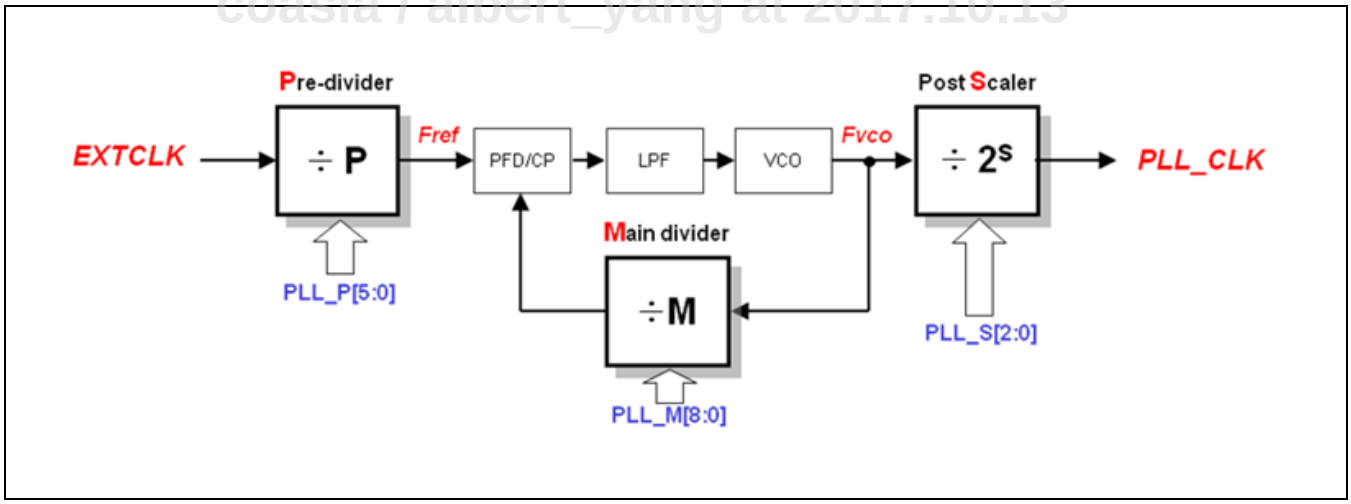


Figure 19 SYSTEM PLL Frequency Synthesis

$$PLL\_CLK = EXTCLK \times \left[\frac{M}{P} \times \frac{1}{2^S} \right]$$

Table 9 SYSTEM PLL Component Output Frequency

Parameter	Min.	Typ.	Max.	Unit	Remarks
Input frequency range	6	–	32	MHz	EXTCLK frequency range
Reference frequency range	6	–	12	MHz	Output of pre divider. (Fref)
VCO frequency range	500	–	1000	MHz	Output of PLL multiplier VCO oscillation range. (Fvco)
PLL output frequency range	31.25	–	1000	MHz	Output of PLL post scaler Minimum value is only for test. (S ≥ 4)

NOTE: For more information about PLL and clock system control, refer to application note.

5.6.2 Master Clock Waveform Diagram

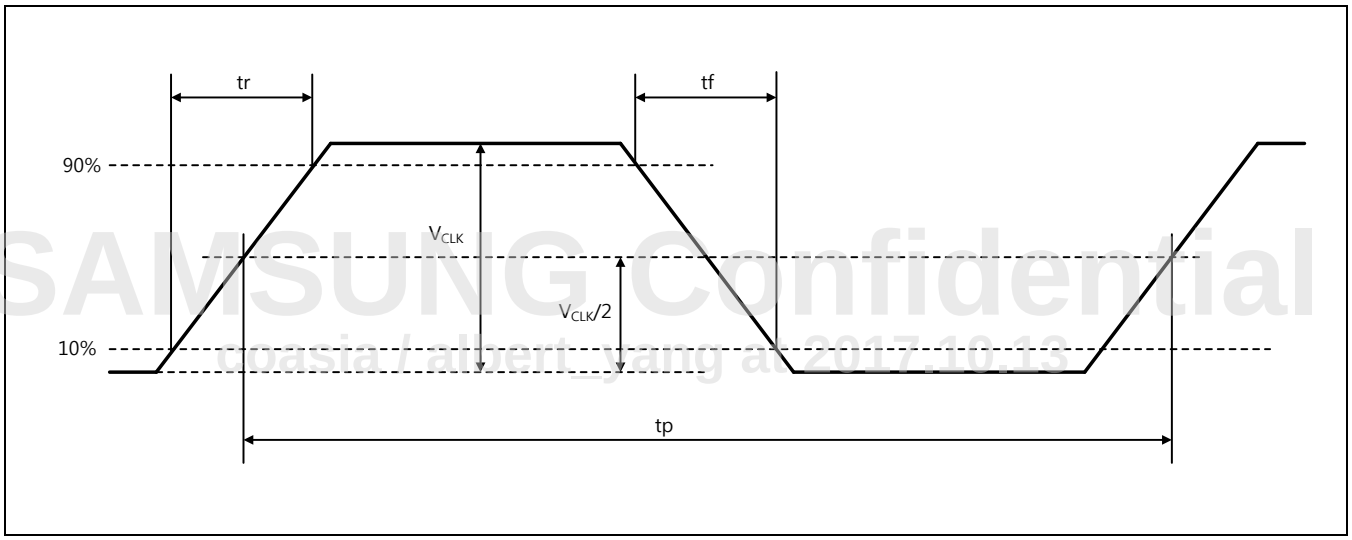


Figure 20 EXTCLK Waveform Diagram

Table 10 EXTCLK Timing Specifications

Parameter	Symbol	Min.	Typ.	Max.	Unit	Comment
EXTCLK clock frequency	EXTCLK	6	–	32	MHz	–
EXTCLK amplitude	VCLK	1.7	1.8	1.9	V	VDDIO = 1.8 V
EXTCLK period	tp	31.25	–	166.7	nsec	–
EXTCLK rise/fall time	tr, tf	–	–	10	nsec	–
EXTCLK jitter	Tjitter	–	–	400	ps	Short term

5.7 Gain Control

5.7.1 Analog Gain Control

Use the following formula to calculate the analog gain :

$$gain = \frac{x}{0x20}$$

NOTE: In S5K3L6XX, analog gain is global; there is no per-channel gain. $gain = \frac{x}{32}$
Gain is supported up to X16.

We can also control the divider (default value is 0x20) and multiply it by 2^N.

N is controlled by the registers described in Table 11.

Table 11 Analog Gain Examples

Gain Value	Analogue_gain_code_global Register Value
X1	0x0020
X2	0x0040
X3	0x0060
X8	0x0100
X10	0x0140
X12	0x0180
X16	0x0200

5.8 NVM OTP Memory

NVM memory module is a non-volatile One-Timing Programming (OTP) memory module. This module enables the saving of unique data to each chip at the production stage.

OTP memory is used to store the following information:

- Chip ID data – Production history data to be stored during die sorting
- Parameter for Lens shading
- 3.5 K bits for users

5.9 Test Pattern

S5K3L6XX may be configured to generate deterministic test patterns. Refer to the application note.

5.10 Output Data Interface

S5K3L6XX MIPI CSI-2 interface is a four-lane high-speed serial interface that connects the camera sensor to a host processor. Maximum bitrate of MIPI of S5K3L6XX is 1.25 Gbps per lane.

S5K3L6XX supports all mandatory requirements in MIPI CSI-2 version 1.00 and DPHY 0.9 specifications. Please see MIPI DPHY 0.9 specification for details.

6 Electrical Characteristics

6.1 Absolute Maximum Rating

Table 12 Absolute Maximum Rating

Description	Symbol	Min.	Typ.	Max.	Unit
Digital absolute maximum (1)	VDDD (max.)	–0.5	–	1.5	V
Analog absolute maximum (2)	VDDA (max.)	–0.3	–	4	V
Special IO absolute maximum (3)	VIO (max.)	–0.3	–	3.6	V
Digital input voltages (4)	VIP	–0.3	–	VDDIO + 0.3	V
VCAP analogue voltage	VCAP	-0.3	–	4.2	V
Storage temperature	TSTR	–40	–	85	°C

NOTE:

1. Digital Inputs: MCLK, RSTN, SDO, SDI, SCK, GPIO_1/2/3/4
2. Voltage on external analog capacitors

6.2 Operating Conditions

Table 13 Operating Conditions

Description	Symbol	Min.	Typ.	Max.	Unit
Digital power supply (1)	VDDD	0.95	1.05	1.15	V
Analog power supply (2)	VDDA	2.7	2.8	2.9	V
Special IO supply	VIO	1.7 (or 2.7)	1.8 (or 2.8)	1.9 (or 2.9)	V
Digital input voltages (3)	VIP	0	–	VDDIO	V
VCAP analogue voltage	VCAP	0	–	4.2	V
Test temperature (4)	TTEST	21	23	25	°C
Optimum operating temperature (5)	TOPT	0	–	60	°C
Normal operating temperature (6)	TOPR	–25	–	60	°C
Functional operating temperature (7)	TFUNC	–30	–	70	°C

NOTE:

1. Digital supply tolerances: 1.05 V ± 100 mV
2. Analogue supply tolerances: 2.8 V ± 100 mV
3. Digital inputs: EXTCLK, XSHUTDOWN, SCL, SDA
4. Test temperature: Image quality test conditions
5. Optimum operating temperature(Tj): No visible degradation in image quality
6. Normal operating temperature(Tj): Camera produces acceptable images
7. Functional operating temperature(Tj): Camera fully functional

6.3 DC Characteristics

Table 14 DC Characteristics

(V_{DDD} = 1.05V, V_{DDA} = 2.8 V, V_{IP} = 2.8V, T_j = 60 °C)

Characteristics	Symbol	Condition	Min.	Typ.	Max.	Unit
Input voltage	VIH	–	0.7 × VIP	–	VIP + 0.3	V
	VIL	–	–0.3	–	0.3 × VIP	
Input leakage current	IIL	VIN = VIP or VSS	–10	–	10	μA
High level output voltage	VOH	IOH = –100 μA	VDDIO –0.2	–	–	V
Low level output voltage	VOL	IOL = 100 μA	–	–	0.2	
High-Z output leakage current	IOZ	VOUT = VSS or VDDD	–10	–	10	μA
Input capacitance	CIN	–	–	–	5	pF
Supply current	ISWSBA	Software standby mode analog (2)	–	–	TBD	μA
	ISWSBD	Software standby mode digital (2)	–	–	TBD	mA
	ISTRMD	Streaming mode analog (3) @ 30fps	–	TBD	TBD	mA
		Streaming mode digital (3) @ 30 fps	–	TBD	TBD	mA

NOTE:

1. Hardware standby current - Digital and Analog Power Off is needed.
2. External clock active (6 MHz)
3. Readout of the full raw image at the 30 fps (MIPI 4-lane), CLOAD = 20 pF

6.4 AC Characteristics

Table 15 AC Characteristics

Characteristics	Symbol	Condition	Min.	Typ.	Max.	Unit
External clock frequency (1)	fXCLK	–	6.0	–	32.0	MHz
External clock duty cycle (1)	fXDUTY	–	45	–	55	%
PLL locking time	tLOCK	–	–	–	1000	µs

NOTE:

1. Applied to EXTCLK pin

7 Lens Specification

7.1 Target Chief Ray Angle (CRA)

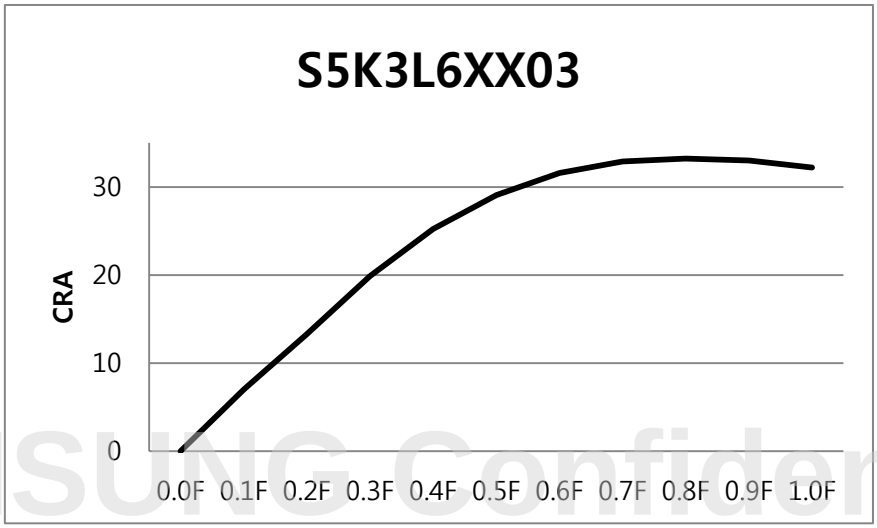


Figure 21 Target CRA

Table 16 Image Height (Field)

Image Height	mm	CRA (deg)
0	0	0
0.1	0.293	7
0.2	0.587	13.3
0.3	0.88	19.9
0.4	1.173	25.23
0.5	1.467	29.08
0.6	1.76	31.6
0.7	2.053	32.91
0.8	2.347	33.25
0.9	2.64	33
1	2.934	32.2

8 Register Description

This section describes S5K3L6XX register map.

Vendor registers are defined for extended functionality control.

8.1 Configuration Registers 1

Table 17 Configuration Register 1

[0x0000 to 0x00FF]

Index	Reset Value	Bit	Register Name	Type	Description
0x0000	0x30	[15:8]	model_id	R	Camera module model identification number
0x0001	0xC6	[7:0]			
0x0002	0x00	[7:0]	revision_number	R	Revision identifier
0x0003	0x00	[7:0]	manufacturer_id	R	Module manufactures code
0x0005	0xFF	[7:0]	frame_count	R	8-bit (0-255) Frame counter value Increment by 1 at the start of each frame
0x0006	0x00	[7:0]	pixel_order	R	0 = Gr, 1 = R, 2 = B, 3 = Gb
0x0008	0x00	[15:8]	data_pedestal	R	Data pedestal: Typically code 64 for 10-bit systems
0x0009	0x40	[7:0]			
0x0040	0x02	[7:0]	frame_format_model_type	R	0x02: 4 Byte Generic Frame Format
0x0041	0x12	[7:0]	frame_format_model_subtype	R	The number of column and row of descriptors used to describe the frame format
0x0042	0x5A	[15:8]	frame_format_descriptor_0	R	{4'h5,x_output_size[11:0]}
0x0043	0x30	[7:0]			
0x0044	0x10	[15:8]	frame_format_descriptor_1	R	{4'h1, Embedded data line[11:0]}
0x0045	0x00	[7:0]			
0x0046	0x57	[15:8]	frame_format_descriptor_2	R	{4'h5,y_output_size[11:0]}
0x0047	0xA8	[7:0]			
0x0080	0x00	[15:8]	analogue_gain_capability	R	Analogue Gain Capability 0 = Single global analogue gain only
0x0081	0x00	[7:0]			
0x0084	0x00	[15:8]	analogue_gain_code_min	R	Minimum recommended analogue gain code
0x0085	0x20	[7:0]			

Index	Reset Value	Bit	Register Name	Type	Description
					Format: 16-bit unsigned integer
0x0086	0x02	[15:8]	analogue_gain_code_max	R	Maximum recommended analogue gain code Format: 16-bit unsigned integer
0x0087	0x00	[7:0]			
0x0088	0x00	[15:8]	analogue_gain_code_step	R	Analogue gain code step size Format : 16-bit unsigned integer
0x0089	0x01	[7:0]			
0x008A	0x00	[15:8]	analogue_gain_type	R	Analogue gain type Format: 16-bit unsigned integer
0x008B	0x00	[7:0]			
0x008C	0x00	[15:8]	analogue_gain_m0	R	Analogue gain m0 constant Format: 16-bit signed integer
0x008D	0x01	[7:0]			
0x008E	0x00	[15:8]	analogue_gain_c0	R	Analogue gain c0 constant Format: 16-bit signed integer
0x008F	0x00	[7:0]			
0x0090	0x00	[15:8]	analogue_gain_m1	R	Analogue gain m1 constant Format: 16-bit signed integer
0x0091	0x00	[7:0]			
0x0092	0x00	[15:8]	analogue_gain_c1	R	Analogue gain c1 constant Format: 16-bit signed integer
0x0093	0x20	[7:0]			
0x00C0	0x01	[7:0]	data_format_model_type	R	0x01: 2-byte Data Format
0x00C1	0x03	[7:0]	data_format_model_subtype	R	Contains the number of data format descriptors used
0x00C2	0x0A	[15:8]	data_format_descriptor_0	R	ex) 0x0A0A: Top 10-bit transmitted as RAW10
0x00C3	0x0A	[7:0]			
0x00C6	0x08	[15:8]	data_format_descriptor_2	R	ex) 0x0808: Top 8-bit transmitted as RAW8
0x00C7	0x08	[7:0]			

8.2 Configuration Registers 2

Table 18 Configuration Register 2

[0x0100 to 0x04FF]

Index	Reset Value	Bit	Register Name	Type	Description
0x0100	0x00	[7:1]	Reserved	R	
		[0]	mode_select	RW	Mode Select 0 = Software Standby 1 = Streaming
0x0101	0x00	[7:2]	Reserved	R	
		[1:0]	image_orientation	RW	Image orientation i.e. horizontal mirror and vertical flip
0x0103	0x00	[7:1]	Reserved	R	
		[0]	software_reset	RW	Software reset
0x0104	0x00	R	Reserved	R	
		[0]	grouped_parameter_hold	RW	The grouped parameter hold register disables the consumption of integration, gain and video timing parameters 0 = Consume as normal 1 = Hold
0x0105	0x00	[7:1]	Reserved	R	
		[0]	mask_corrupted_frames	RW	Refer to Integration Time and Gain Control Chapter
0x0106	0x00	[7:1]	Reserved	R	
		[0]	fast_standby_ctrl	RW	0 – Frame completes before mode entry 1 – Frame may be truncated before mode entry
0x0107	0xAC	[7:0]	cci_address_control	RW	Expressed as 8bit / Slave ID register
0x0108	0x00	[7:0]	2nd_cci_if_control	RW	[0] 1 = enable 2nd CCI Interface, 0 = disable 2nd CCI Interface [1] 1 = enable ACK for 2nd CCI interface, 0 = disable ACK for 2nd CCI interface
0x0109	0x6C	[7:0]	2nd_cci_address_control	RW	2nd Slave ID register, expressed as 8bit
0x0110	0x00	[7:4]	Reserved	R	
		[3:0]	channel_identifier	RW	Valid range: 0 to 3 for CSI-2 Default value 0
0x0111	0x02	[7:2]	Reserved	R	
		[1:0]	signalling_mode	RW	0,1 = Reserved

Index	Reset Value	Bit	Register Name	Type	Description
					2 = CSI-2
0x0112	0x0A	[15:8]	data_format	RW	Output Data Format 0x0808: RAW8 0x0A0A: RAW10 (default)
0x0113	0x0A	[7:0]			
0x0114	0x01	[7:0]	lane_mode	RW	3 = 4-lane (default)
0x0120	0x00	[7:1]	Reserved	R	
		[0]	gain_mode	RW	0 = Global Analogue Gain (Default) 1 = Per Channel Analogue Gain (Only if sensor supports it),
0x0136	0x18	[15:8]	Extclk_frequency_mhz	RW	Nominal EXTCLK frequency (8.8 fixed point number)
0x0137	0x00	[7:0]		RW	
0x0200	0x00	[15:8]	fine_integration_time	RW	Fine integration time (pixels) Format: 16-bit unsigned integer
0x0201	0x00	[7:0]			
0x0202	0x03	[15:8]	coarse_integration_time	RW	Coarse integration time (lines) Format: 16-bit unsigned integer
0x0203	0xDE	[7:0]			
0x0204	0x00	[15:8]	analogue_gain_code_global	RW	Global Analogue Gain Code Format: 16-bit unsigned integer
0x0205	0x20	[7:0]			
0x020E	0x01	[15:12]	Reserved	R	
		[11:8]	digital_gain_global	RW	Global channel digital gain value Format: 16-bit unsigned iReal
0x020F	0x00	[7:0]			
0x0301	0x06	[7:4]	Reserved	R	
		[3:0]	vt_pix_clk_div	RW	Video Timing Pixel Clock Divider Value Format: 16-bit unsigned integer
0x0305	0x04	[7:6]	Reserved	R	
		[5:0]	pre_pll_clk_div	RW	System Pre PLL clock Divider Value Format: 16-bit unsigned integer
0x0306	0x00	[15:10]	Reserved	R	
		[9:8]	pll_multiplier	RW	System PLL multiplier Value Format: 16-bit unsigned integer
0x0307	0x78	[7:0]			
0x030C	0x00	[15:8]	op_pre_pll_clk_div	RW	Pre PLL clock Divider Value Format: 16-bit unsigned integer
0x030D	0x04	[7:0]			
0x030E	0x00	[15:8]	op_pll_multiplier	RW	Pre PLL multiplier Value Format: 16-bit unsigned integer
0x030F	0x64	[7:0]			
0x3C1C	0xC5	[7:4]	Reserved	RW	
		[3:0]	reg_div_dbr	RW	Clock divider for DBLR clock
0x0340	0x0C	[15:8]	frame_length_lines	RW	Frame Length Format: 16-bit unsigned integer
0x0341	0xBC	[7:0]			

Index	Reset Value	Bit	Register Name	Type	Description
					(Lines)
0x0342	0x13	[15:8]	line_length_pck	RW	Line Length Format: 16-bit unsigned integer (Pixel Clocks)
0x0343	0x20	[7:0]			
0x0344	0x00	[15:13]	Reserved	RW	
		[12:8]	x_addr_start	RW	X-address of the top left corner of the visible pixel data Format: 16-bit unsigned integer (Pixels)
0x0345	0x08	[7:0]			
0x0346	0x00	[15:12]	Reserved	R	
		[11:8]	y_addr_start	RW	Y-address of the top left corner of the visible pixel data Format: 16-bit unsigned integer (Lines)
0x0347	0x08	[7:0]			
0x0348	0x10	[15:13]	Reserved	R	
		[12:8]	x_addr_end	RW	X-address of the bottom right corner of the visible pixel data Format: 16-bit unsigned integer (Pixels)
0x0349	0x77	[7:0]			
0x034A	0x0C	[15:12]	Reserved	R	
		[11:8]	y_addr_end	RW	Y-address of the bottom right corner of the visible pixel data Format: 16-bit unsigned integer (Lines)
0x034B	0x37	[7:0]			
0x034C	0x10	[15:13]	Reserved	R	
		[12:8]	x_output_size	RW	Width of image data output from the sensor module Format: 16-bit unsigned integer (Pixels)
0x034D	0x70	[7:0]			
0x034E	0x0C	[15:12]	Reserved	R	
		[11:8]	y_output_size	RW	Height of image data output from the sensor module Format: 16-bit unsigned integer (Lines)
0x034F	0x30	[7:0]			
0x0381	0x01	[7:5]	Reserved	R	
		[4:0]	x_even_inc	RW	Increment for even pixels: 0, 2, 4 etc Format: 16-bit unsigned integer
0x0383	0x01	[7:5]	Reserved	R	
		[4:0]	x_odd_inc	RW	Increment for odd pixels: 1, 3, 5 etc Format: 16-bit unsigned integer
0x0385	0x01	[7:5]	Reserved	R	
		[4:0]	y_even_inc	RW	Increment for even pixels: 0, 2, 4 etc Format: 16-bit unsigned integer

Index	Reset Value	Bit	Register Name	Type	Description
0x0387	0x01	[7:5]	Reserved	R	
		[4:0]	y_odd_inc	RW	Increment for odd pixels: 1, 3, 5 etc Format: 16-bit unsigned integer

8.3 Configuration Registers 3

Table 19 Configuration Register 3

[0x0600 to 0x0FFF]

Index	Reset Value	Bits	Register Name	Type	Description
0x0601	0x00	[7:3]	Reserved	R	
		[2:0]	test_pattern_mode	RW	0 = No pattern(default) 1 = Solid color 2 = Full color bar 3 = Fade to grey color bar
0x0602	0x02	[15:10]	Reserved	R	
		[9:8]	test_data_red	RW	R pixel value for 1-color frame mode
0x0603	0x00	[7:0]			
0x0604	0x02	[15:10]	Reserved	R	
		[9:8]	test_data_greenR	RW	Gr pixel value for 1-color frame mode
0x0605	0x00	[7:0]			
0x0606	0x02	[15:10]	Reserved	R	
		[9:8]	test_data_blue	RW	B pixel value for 1-color frame mode
0x0607	0x00	[7:0]			
0x0608	0x02	[15:10]	Reserved	R	
		[9:8]	test_data_greenB	RW	Gb pixel value for 1-color frame mode
0x0609	0x00	[7:0]			
0x060A	0x00	[15:12]	Reserved	R	
		[11:8]	horizontal_cursor_width	RW	Defines the width of the horizontal cursor (in pixels)
0x060B	0x00	[7:0]			
0x060C	0x01	[15:12]	Reserved	R	
		[11:8]	horizontal_cursor_position	RW	Defines the top edge of the horizontal cursor
0x060D	0x00	[7:0]			
0x060E	0x00	[15:12]	Reserved	R	
		[11:8]	vertical_cursor_width	RW	Defines the width of the vertical cursor (in pixels)
0x060F	0x00	[7:0]			
0x0610	0x00	[15:8]	vertical_cursor_position	RW	Defines the left hand edge of the vertical cursor.
0x0611	0x00	[7:0]			
0x0820	0x04	[31:24]	requested_link_rate	RW	Target Frequency per MIPI data lane (16.16 fixed point number)
0x0821	0xB0	[23:16]			
0x0822	0x00	[15:8]			
0x0823	0x00	[7:0]			
0x0900	0x00	[7:0]	binning_mode	RW	0 = Disabled, 1 = Enabled

Index	Reset Value	Bits	Register Name	Type	Description
0x0901	0x00	[7:0]	binning_type	RW	High nibble specifies Column Binning factor Low nibble specifies Row Binning factor